Massachusetts Institute of Technology

Laboratory for Electromagnetic and Electronic Systems

High frequency ac-dc converter

# Miniaturized High-Frequency Integrated Power Conversion for Grid Interface

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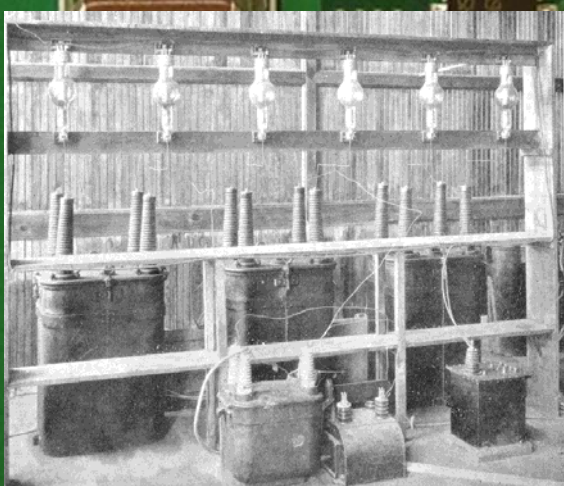
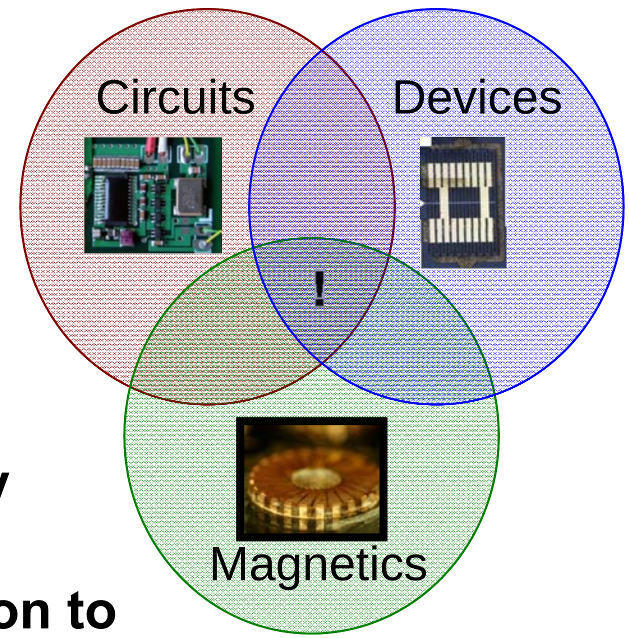


20 kW Kenotron Rectifier, Circa 1926
(From Principles of Rectifier Circuits, Prince and Vogdes, McGraw Hill 1927)

Commercial LED Driver Rectifier, Circa 2012

??

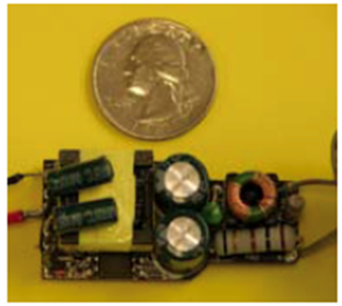
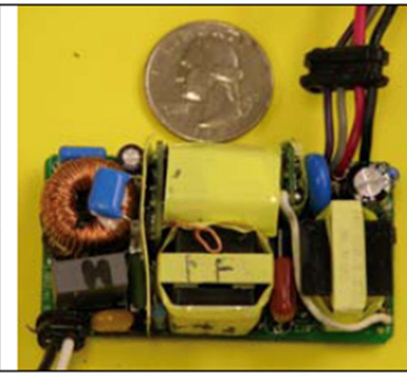
- **Investigate the use of greatly increased switching frequencies to miniaturize *low-power, grid-interface* converters**
  - **HF frequency range, 3-30 MHz, 10-100x conventional**
  - **LED driver as an example**




- **PowerChip Team (ARPA-E ADEPT)**

- **This talk describes:**
  1. **Application considerations and frequency constraints in this space**
  2. **System architecture and topology selection to address these considerations and constraints**
  3. **Design and performance of an experimental prototype demonstrating the proposed approach (Operation at 5-10 MHz at > 50 W/in$^3$)**

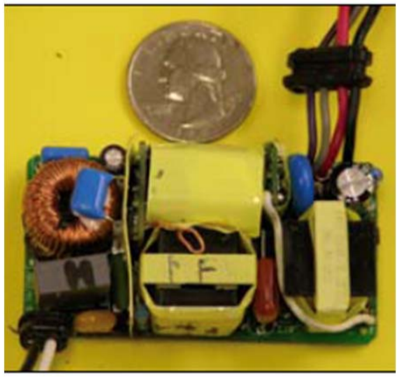
# Example: Solid-State Lighting Drivers

| Model | Polar-ray 6W |  | Cooper 1200 Series 24.8 W |  |
|---|---|---|---|---|
| Output power | 4.0 W | | 21.1 W | |
| Sw. Frequency | 57 kHz | | 100 kHz | |
| Efficiency | 64% | | 85% | |
| Converter Volume | 1.27 $in^3$ | | 4.76 $in^3$ | |

- **Today: η ~ 60-90%**
- **power density of commercial designs < 5 $W/in^3$**
  - **Switching frequencies < 150 kHz**
  - **Largest components are typically magnetic elements (inductors, transformers)**
  - **Second largest are usually electrolytic capacitors for twice-line-frequency energy storage**
  - **EMI filters also take up significant volume**
- **Power factor / line-frequency energy buffering is also an important consideration**
  - **EnergyStar: PF of 0.7 (residential) or 0.9 (commercial) is desired but mostly NOT achieved**

# Motivations for Frequency Increases

- **Goals**
  - **Miniaturization**
  - **Integration**



**Commercial LED Driver**
**100 kHz**
**21 W**
**85% eff**
**4.8 W/in$^3$**

- **Passive energy storage components (especially magnetics) are the dominant constraint**

- ***Energy storage* requirements vary inversely with frequency: C,L proportional to $f_{sw}^{-1}$**

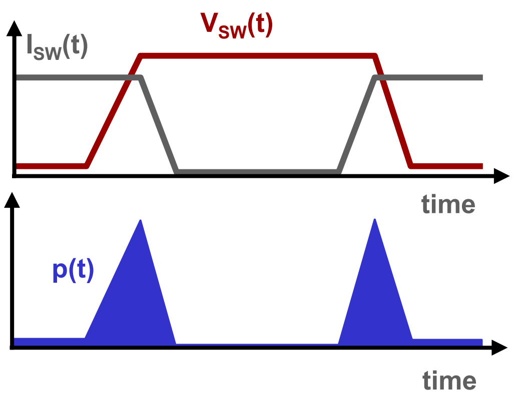
- **Volume can be scaled down with frequency**
  - **But, often scales down *slowly* with frequency**
  - **Magnetic core materials especially impact frequency scaling**
  - **Application constraints are also an important factor**

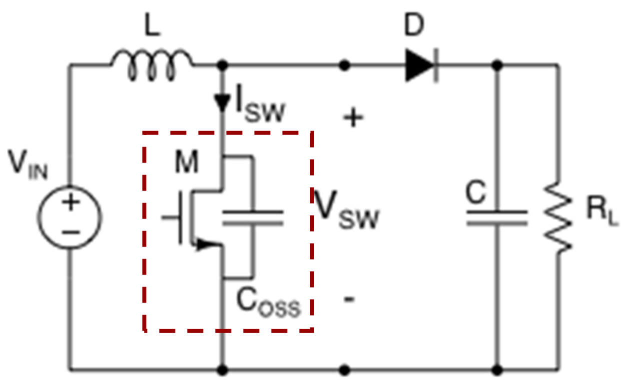
**Perreault, et. al., "Opportunities and Challenges in Very High Frequency Power Conversion," APEC 2009**

# Switching Frequency Limitations: Loss

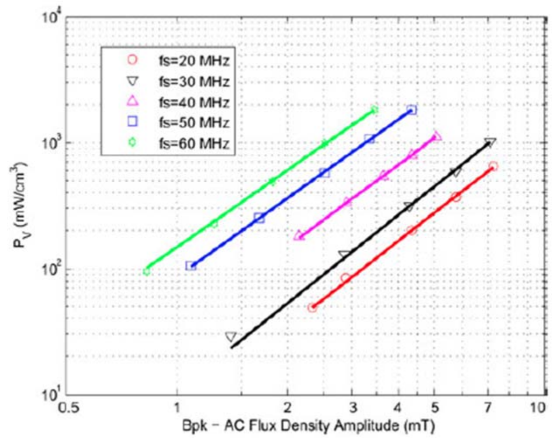
- **Loss mechanisms in power electronics limit switching frequencies**
  - **Relative importance of different losses depends on power, voltage**
  - **For this design space, switching loss and core loss dominate**

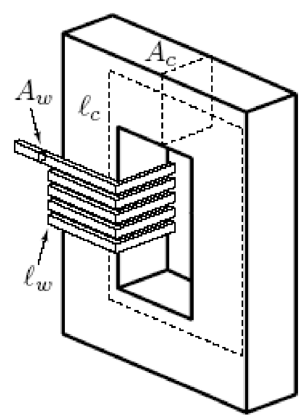
- **Switching loss ($\propto f$)**




- **Magnetic core loss ($\propto f^k$)**

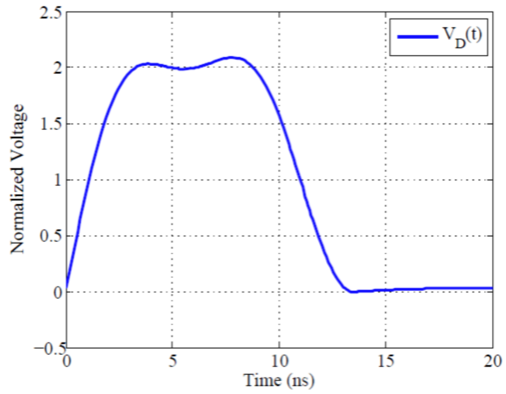


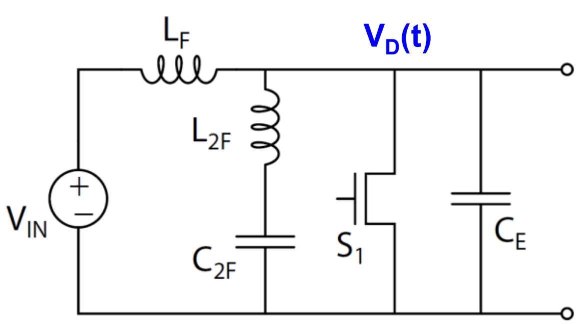



# Switching Frequency Solutions

- **Minimize frequency dependent device loss, switch fast enough to eliminate/minimize magnetic materials, enable PCB integration**

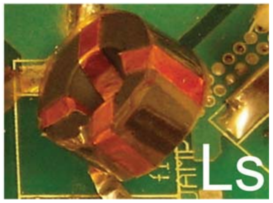
- **ZVS Soft switching**




- **Coreless magnetics in package or substrate**

- **Low-permeability RF magnetic materials**



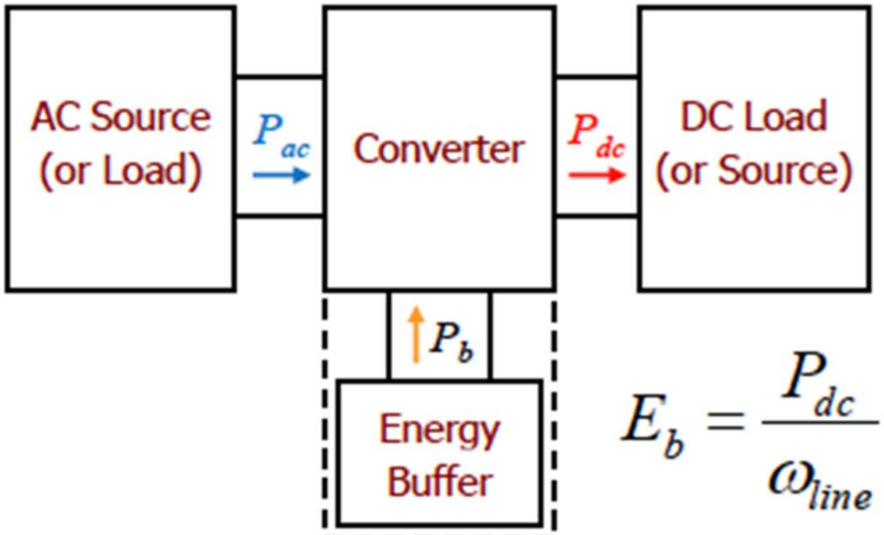
# Design Requirements and Device Capabilities

- **Application requirements also impose limits on miniaturization**
  - **e.g., twice-line-frequency energy buffering requirements for interfacing single-phase ac to dc imposes size constraints**

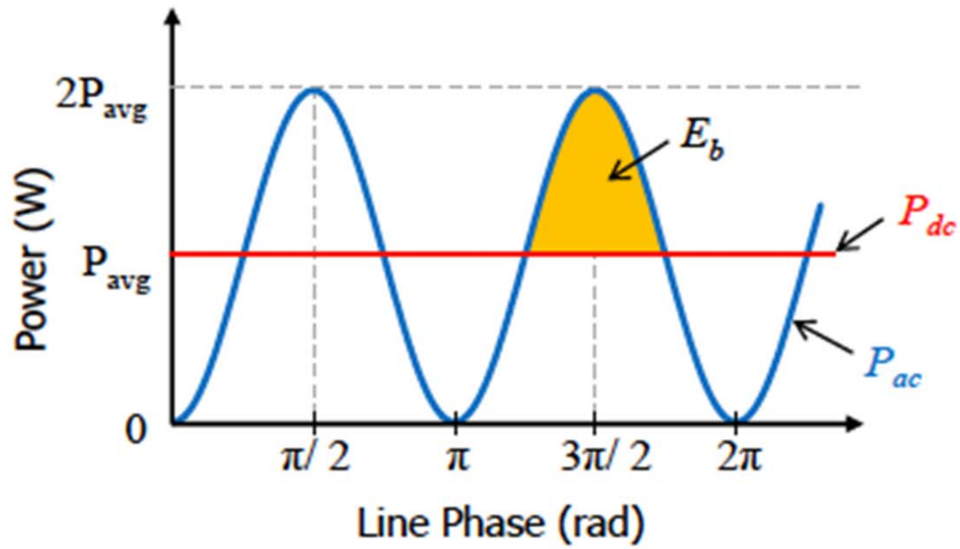
- **Device & component characteristics impact ability to scale frequency and miniaturize, separate from loss**
  - **Component parasitics can limit the ability to scale frequency**
  - **e.g., at high voltage and low power, parasitic capacitance (e.g., device capacitance) imposes constraints**

# Twice-Line-Frequency Energy Buffering

- **Interface between (continuous) dc and single-phase ac requires buffering of twice-line-frequency energy**
  - **Energy storage requirement is independent of switching frequency**




$$E_b = \frac{P_{dc}}{\omega_{line}}$$




- **Electrolytic capacitors are energy dense but have temperature and lifetime limits**

Added Goal: Achieve energy buffering (for high pf and continuous output) at high power density without electrolytics

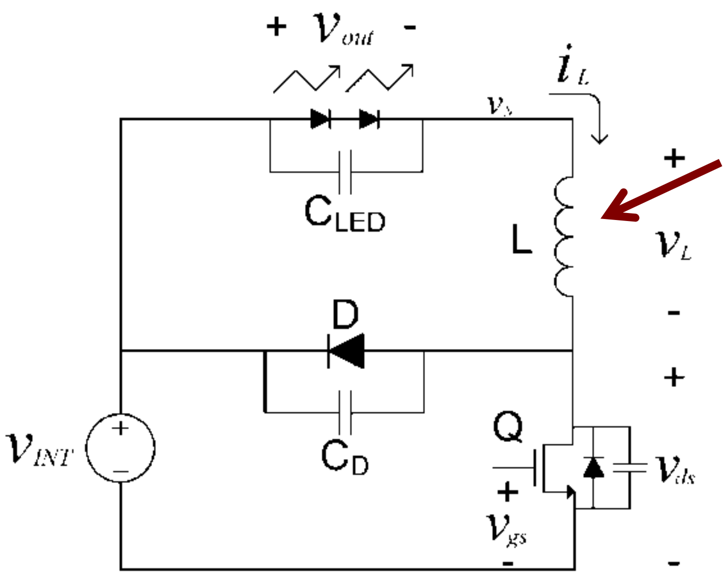
# Application Considerations: LED Drivers

- **Operation from ac-line-voltage inputs (to 200 V peak) to moderate outputs (~30 V) at low powers (~10-50 W)**
  - **Resonant circuits at high voltage and low current lead to small capacitance values and large inductor values**
  - **Increase in frequency reduces both L's, C's**
- ***Minimum practical capacitances can limit frequency***

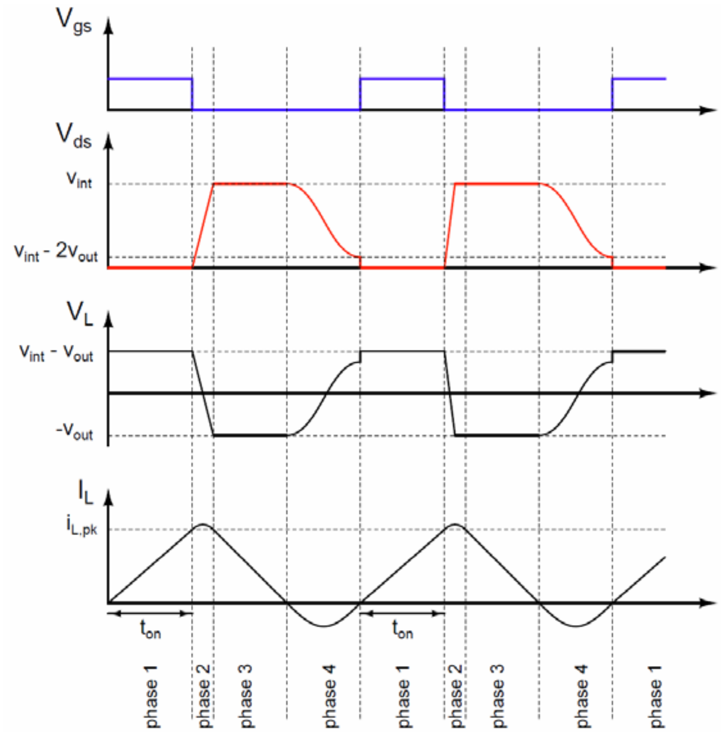
- **Design approach must be selected to require minimal magnetics/larger capacitances to enable greater frequency scaling**
  - **Stacked architectures to reduce subsystem operation voltage**
  - **Multi-stage/merged conversion techniques**
  - **Topologies selected for small magnetics size**

# HF dc-dc Power Stage

- High-frequency dc-dc conversion block (50-100 V in, ~25-40 V out)

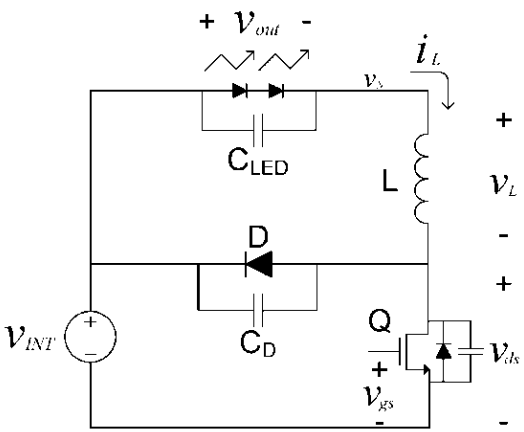


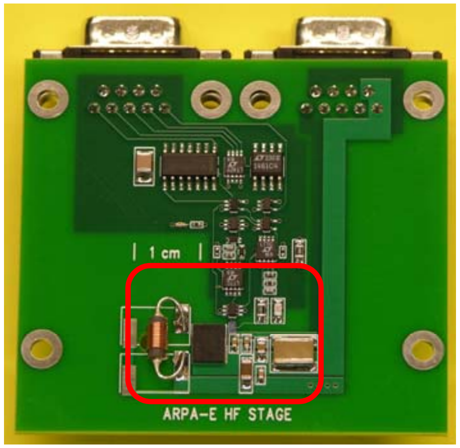

*Enables small Inductance and possible Integration!*




- **Resonant transition inverted buck circuit at edge of DCM**
- **ground referenced switch for HF switching operation (~5-10 MHz)**
- **Low voltage stress enables operation with significant device capacitance**
- **Near-minimum magnetics (700-1000 nH inductor for 100 V input at 10’s of W)**
- **ZVS / near ZVS with PWM “on-time” control of output current**

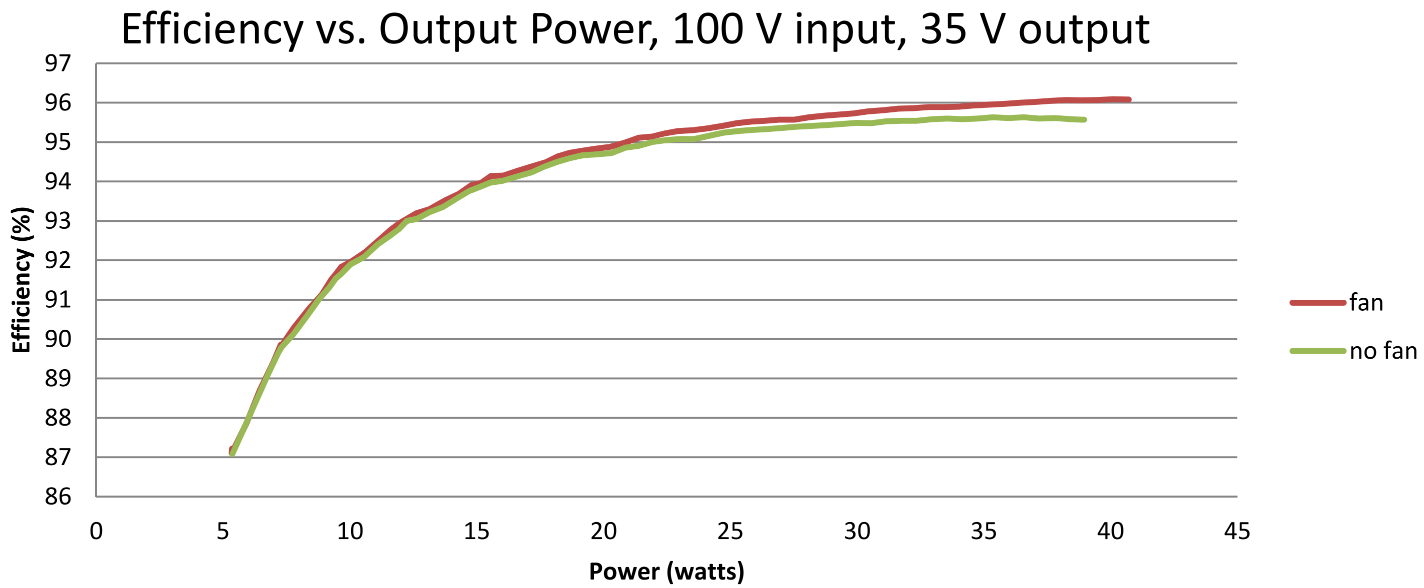
# HF dc-dc Power Stage





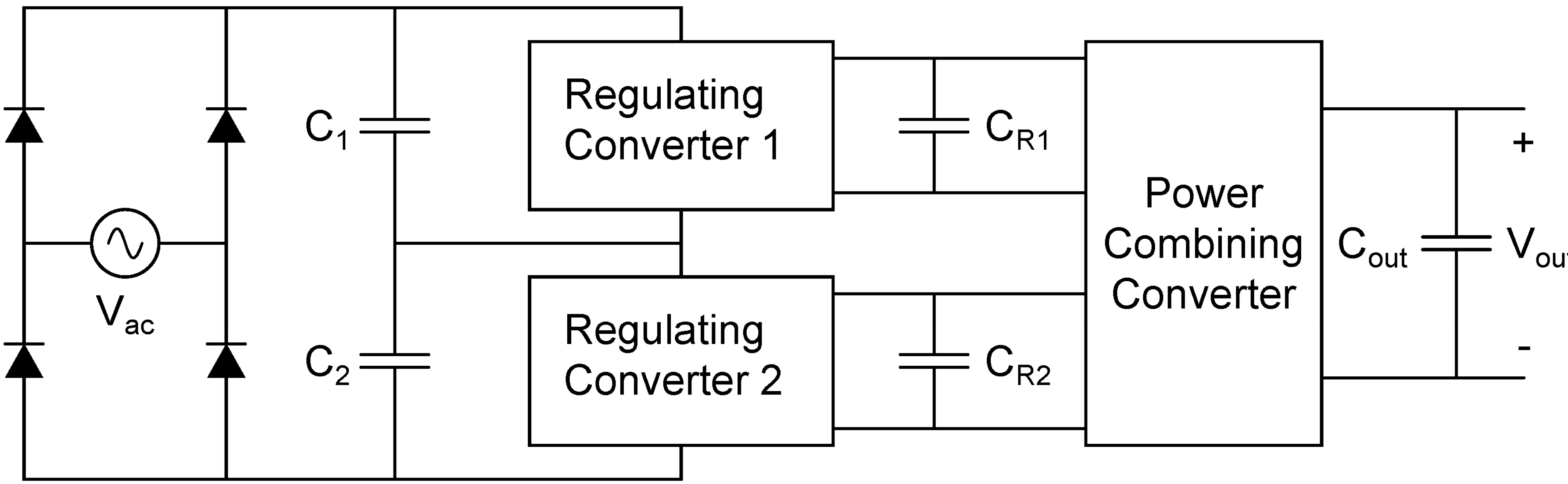
**Discrete Prototype $V_{in}$=100 V, $V_{out}$ = 35 V, $f_{sw}$ ~ 7.8 MHz**



# Architectural Strategy

- **Use a "stacked" circuit architecture to enable processing of high input voltage with lower-voltage blocks**
  - **Enables scaling of individual circuit blocks to higher frequencies**
  - **Utilize "resonant-transition inverted buck" conversion to process energy at high frequency**
- **Buffer line-frequency energy at relatively high voltage with large voltage swing to minimize buffer capacitor size**
  - **Can use film or ceramic capacitors, eliminating electrolytic capacitors while maintaining high power density**
  - **This is important because energy buffering depends upon line frequency, and not upon switching frequency**

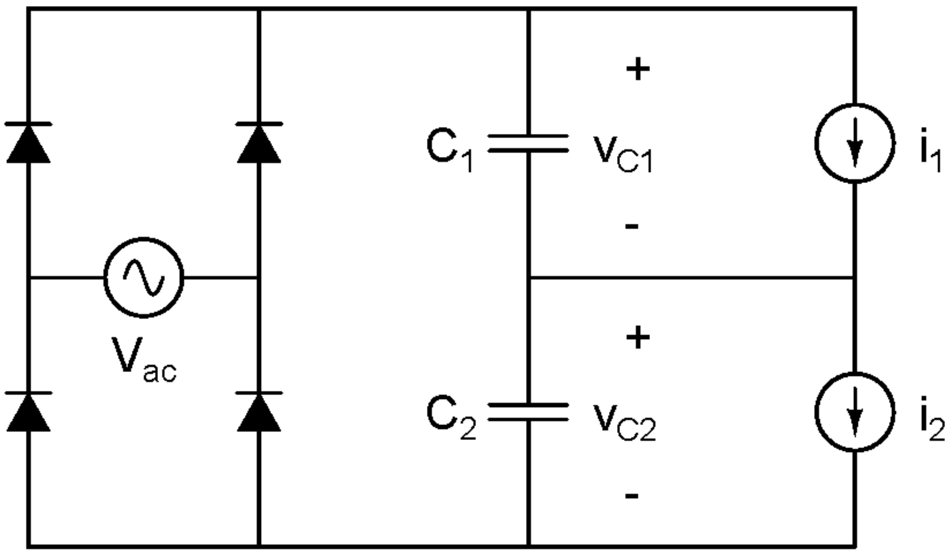
# HF AC-DC Architecture

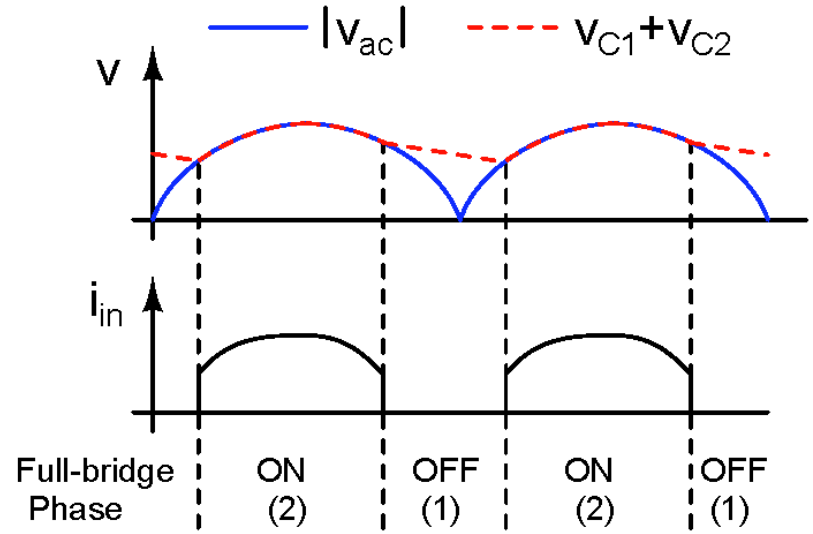



- Two stacked "regulating" converters operating at HF
  - Generate regulated voltages across $C_{R1}$, $C_{R2}$
- Second stage combines power (but doesn't need to regulate)
- Stacking is also used for energy buffering
  - Capacitor $C_2$ (large) buffers twice-line-frequency energy (with high voltage fluctuation over the ac line cycle)
  - Capacitor $C_1$ (small) enables capacitor stack voltage to track line voltage

Lim, et. al., "Power Conversion Architecture for Grid Interface at High Switching Frequency ," APEC 2014

# HF AC-DC Architecture – Front End

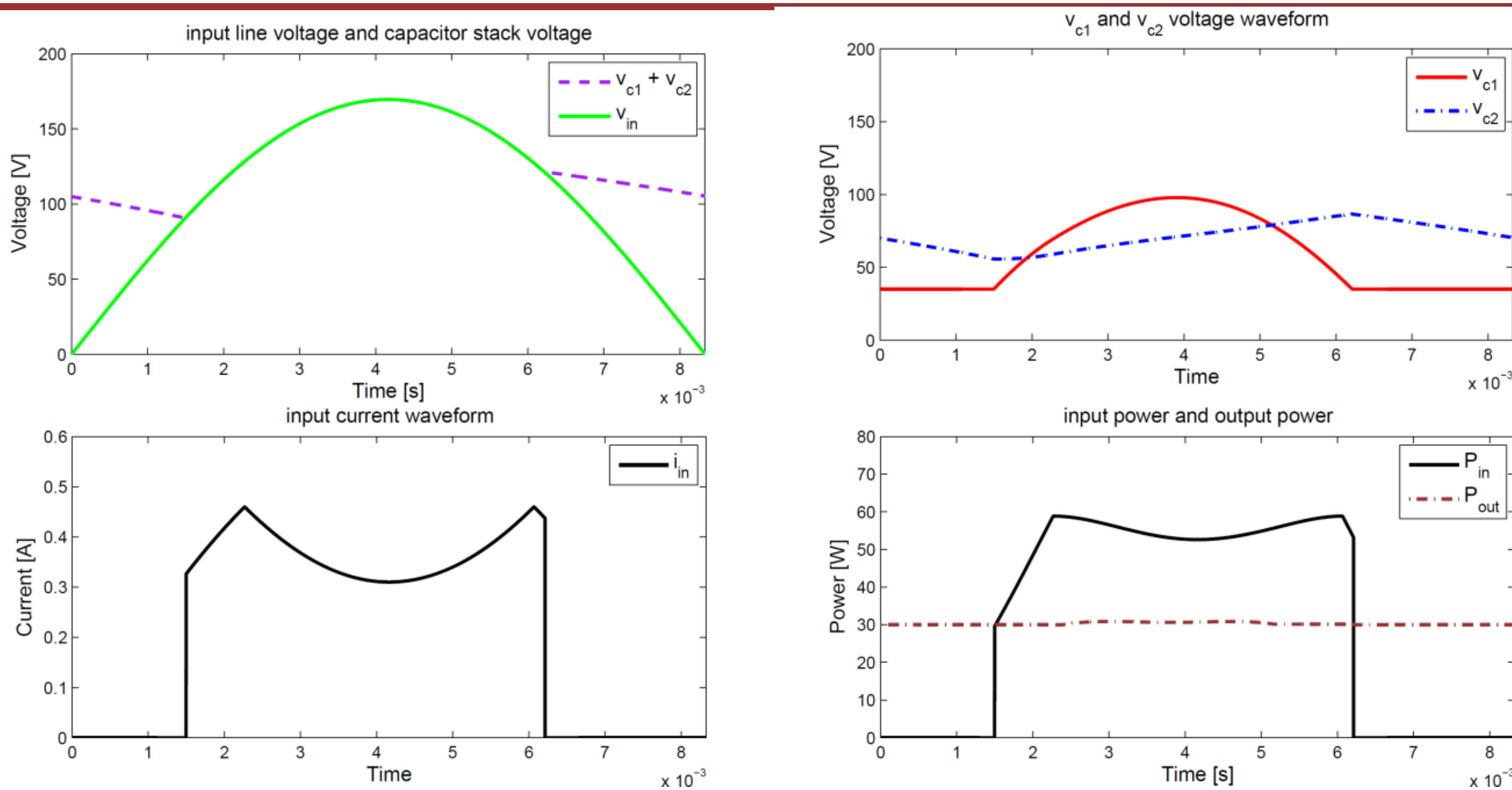



**Control buck power stage currents $i_1$, $i_2$ to:**

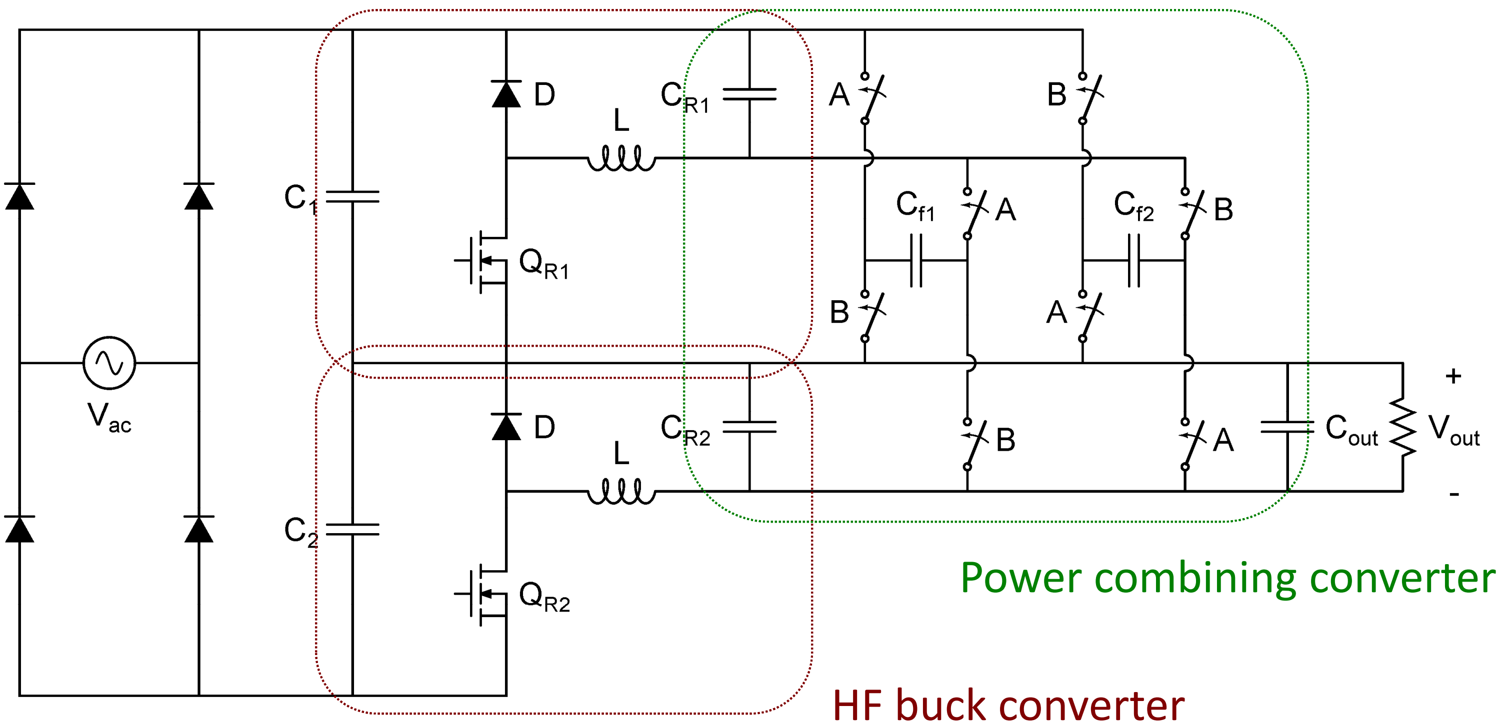
- **Provide desired (constant) total output power**
- **Draw net input current providing high power factor**
  - **Buffer twice-line-frequency energy on $C_2$**
  - **Follow a desired waveform over a limited fraction of the line cycle**
    - **“clipped sine” wave is optimal for highest power factor**

# Stacked Converter Model Simulation



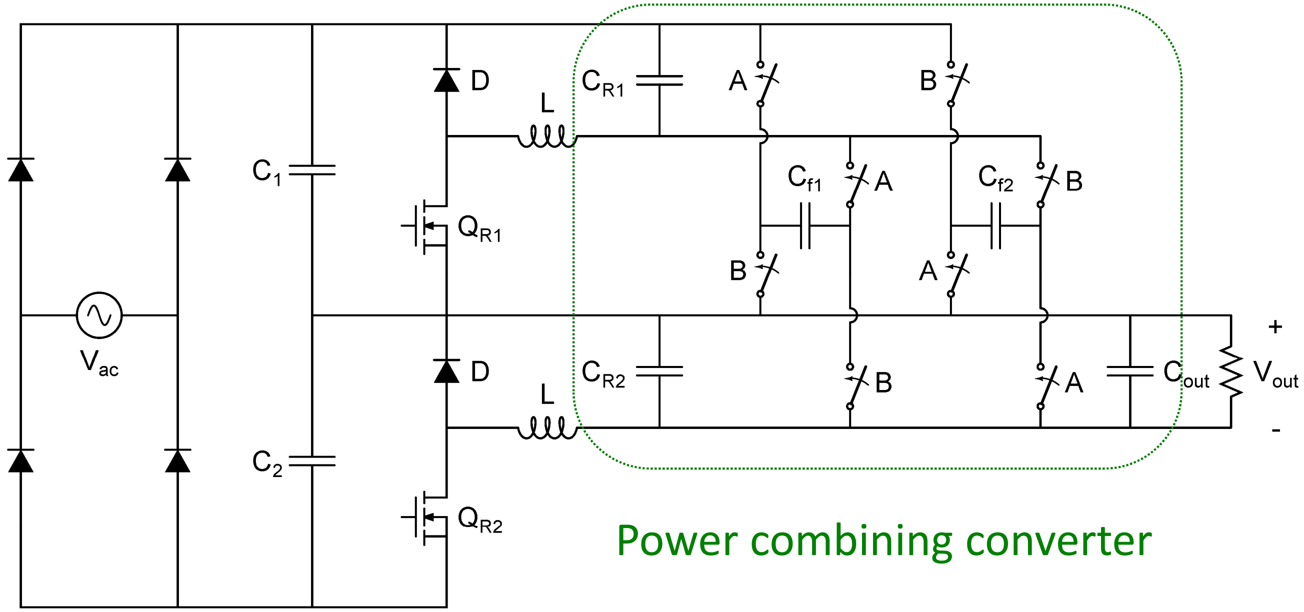

- **Example current and voltage waveforms**
  - **"Clipped-sine with inverted peak" flattens peak power draw while keeping high power factor**
- **Constant output power supplied to load**
  - **Energy buffered on $C_2$ with large "triangular" voltage swing**

# Prototype Converter

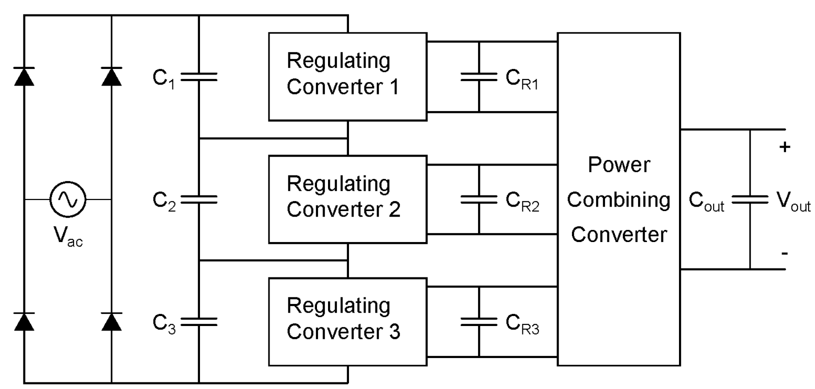



- **Two stacked HF buck converters modulate input power across the ac line cycle, causing desired input current waveform and providing energy buffering in $C_2$**
- **SC circuit combines the power from converters to supply the load**

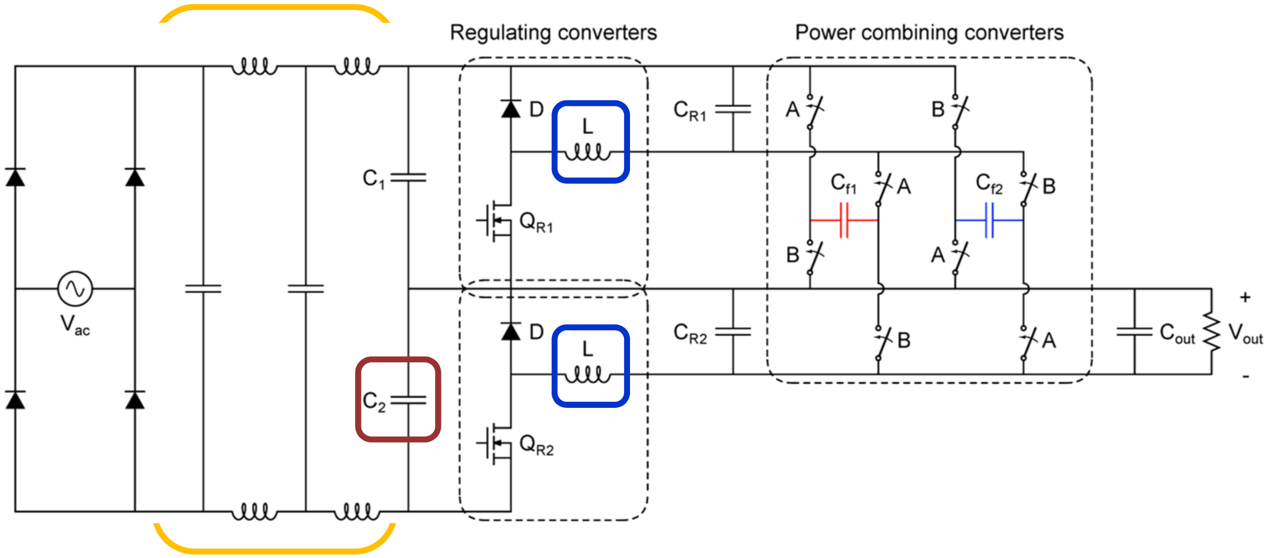
# SC Power Combining Converter

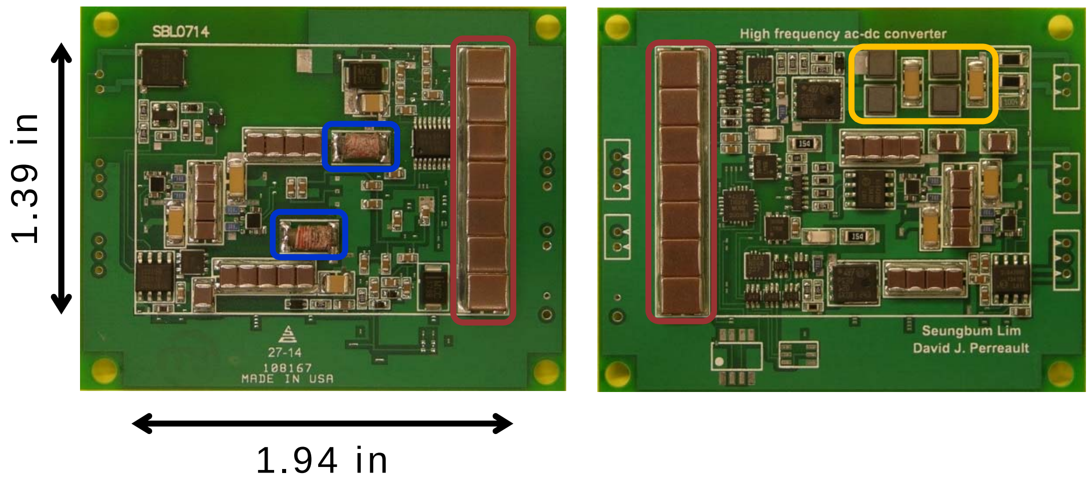



- Interleaved switched capacitor charge transfer circuit
- Delivers power from $C_{r1}$ to $C_{r2}$ (output port)
- Operates at ~30kHz with 50% duty ratio
  - High efficiency operation
- May be expanded:
  - Isolated power combining converters are also possible
  - Universal-input power converters



# Prototype Converter (Gen 2)

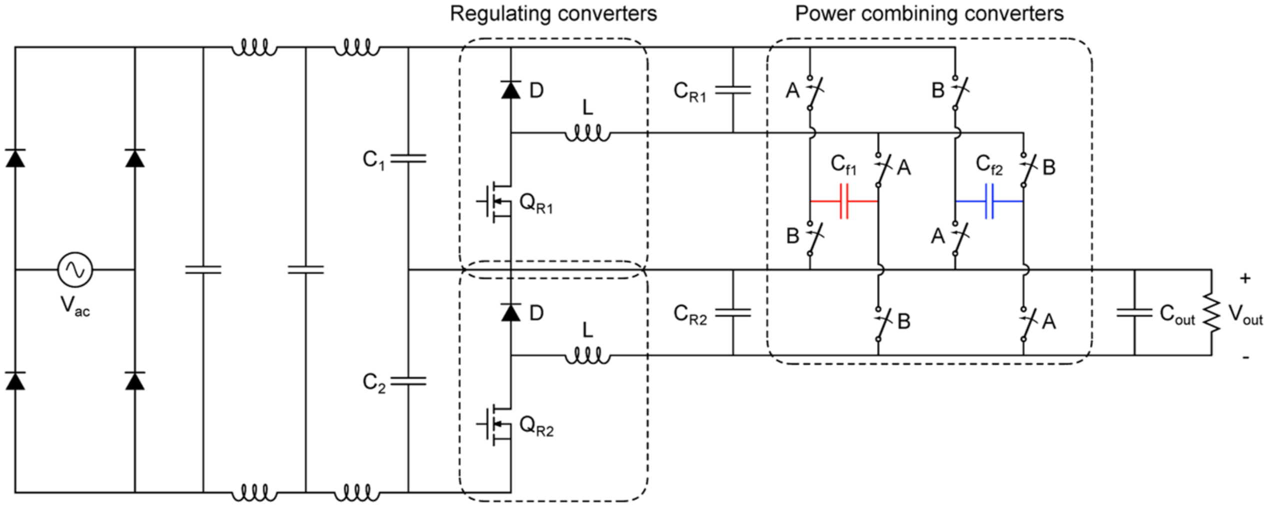



- **Buffer Capacitors**
- **EMI Filter**
- **Inductors**

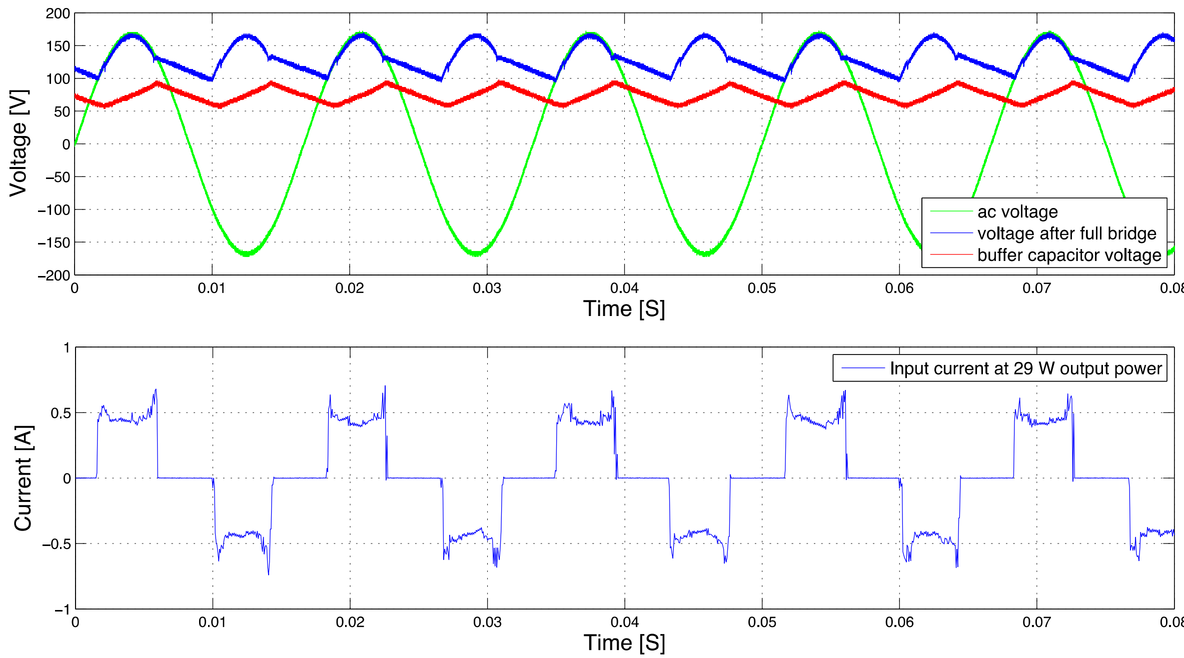
- **120 Vac input, 35 V dc output, >30 W rating**
- **Switching frequency ~ 5-10 MHz (varies across operation)**
- **No electrolytic capacitors!**

# Prototype Converter Details



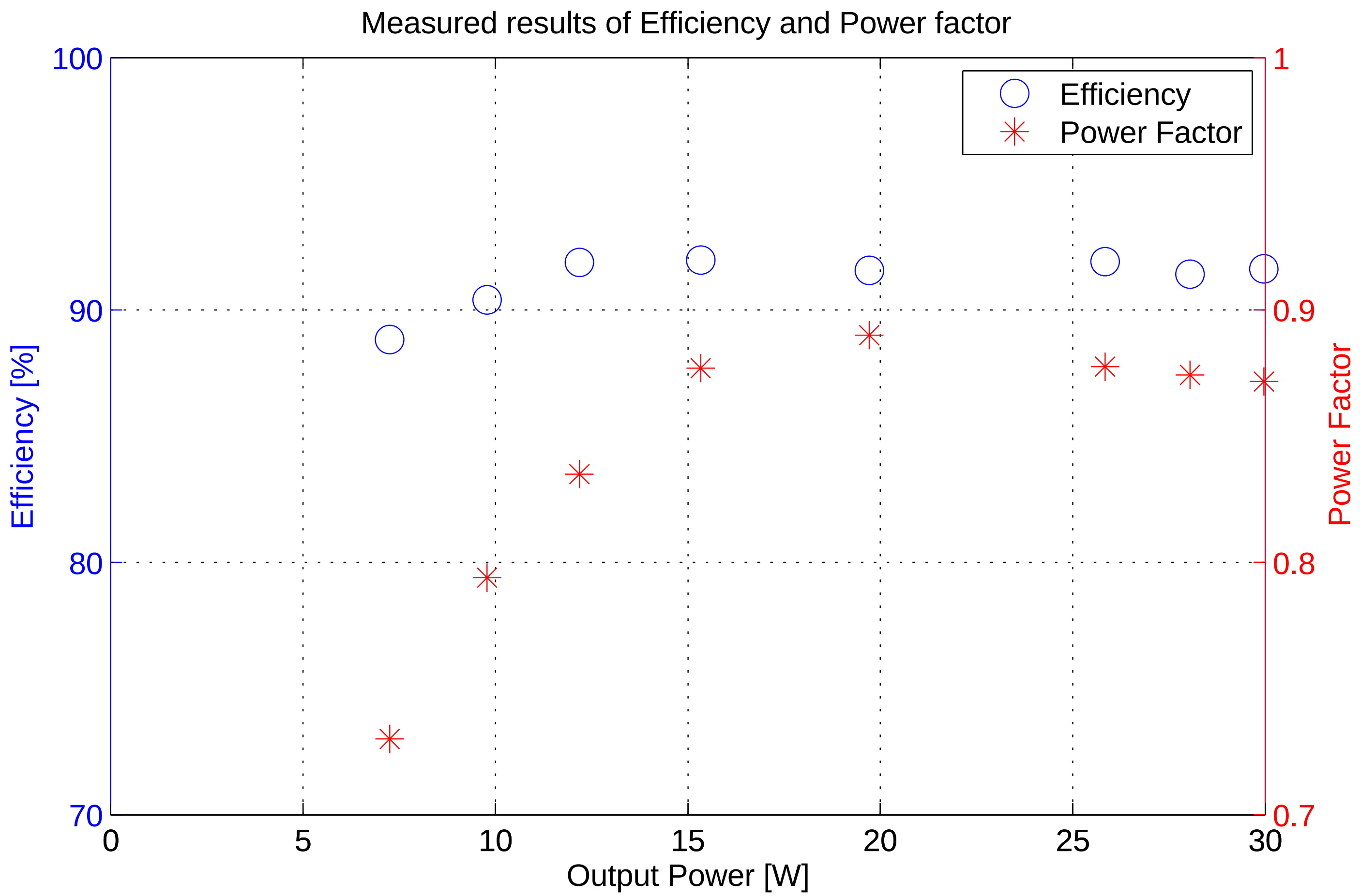

- **Buffer Capacitor: 14  x 15 uF ( X7R 100V, Ceramic TDK)**
- **EMI filter:**
  - **4 x 47 uH inductors (1008PS-473KL, coilcraft)**
  - **2 x 10 nF capacitors ( 200V, X7R ceramic, Kemet)**
- **Regulating converters**
  - **Inductor: 10 turn Litz wire on Micrometals P68-106 core (800 nH)**
  - **Switch: GaN HEMT transistor (EPC 2012, 200V 3A, EPC)**
  - **Diode: Schotky diode (STPS30120, 120V 30 A, ST)**
- **SC circuit**
  - **Switch: GaN HEMT transistor (EPC 2012, 200V 3A, EPC)**

# Experimental Results

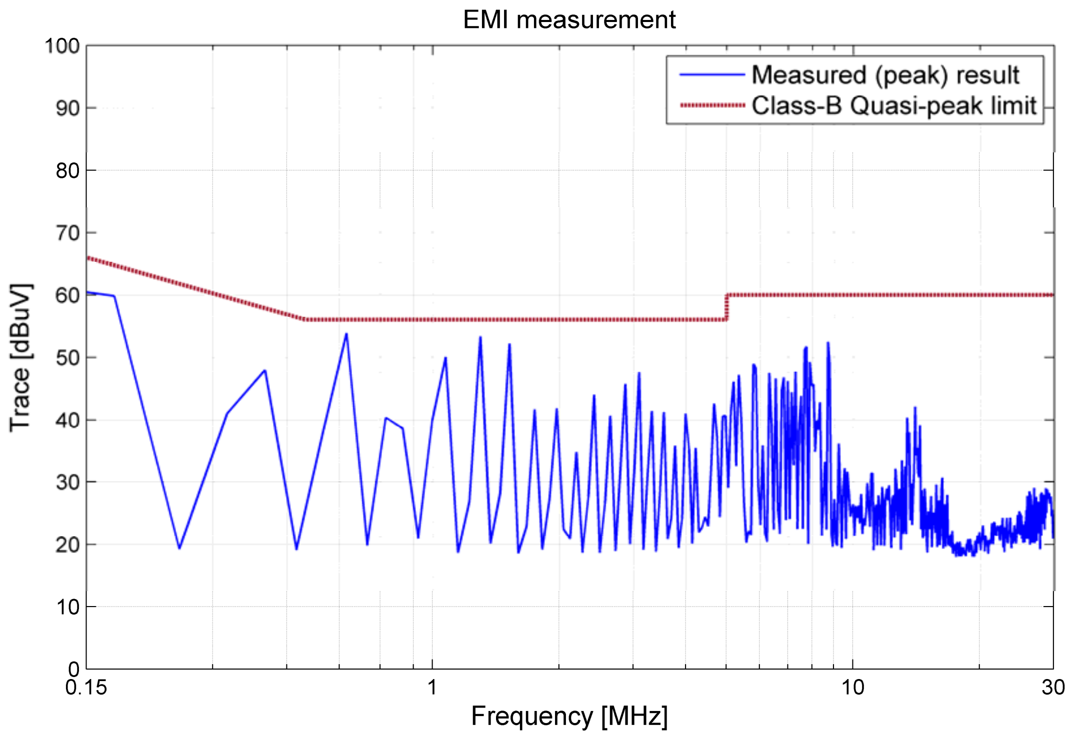



- **Design successfully demonstrates proposed approach**
  - **Operation matches models**
- **High power factor ~0.88 (higher appears possible)**
  - **15uF x 14 = 210 uF MLCC ac energy buffer capacitor (works as ~50 uF at 70V): eliminates electrolytic capacitors at modest size**
- **Efficiency ~92%**

# Performance Across Output Power

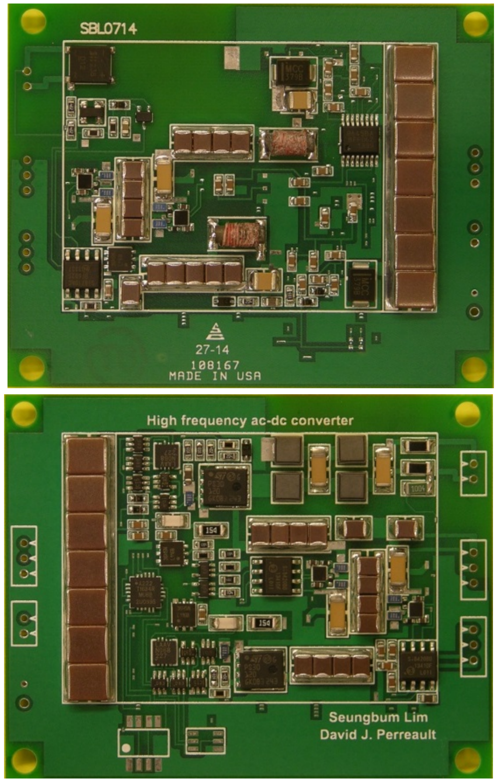


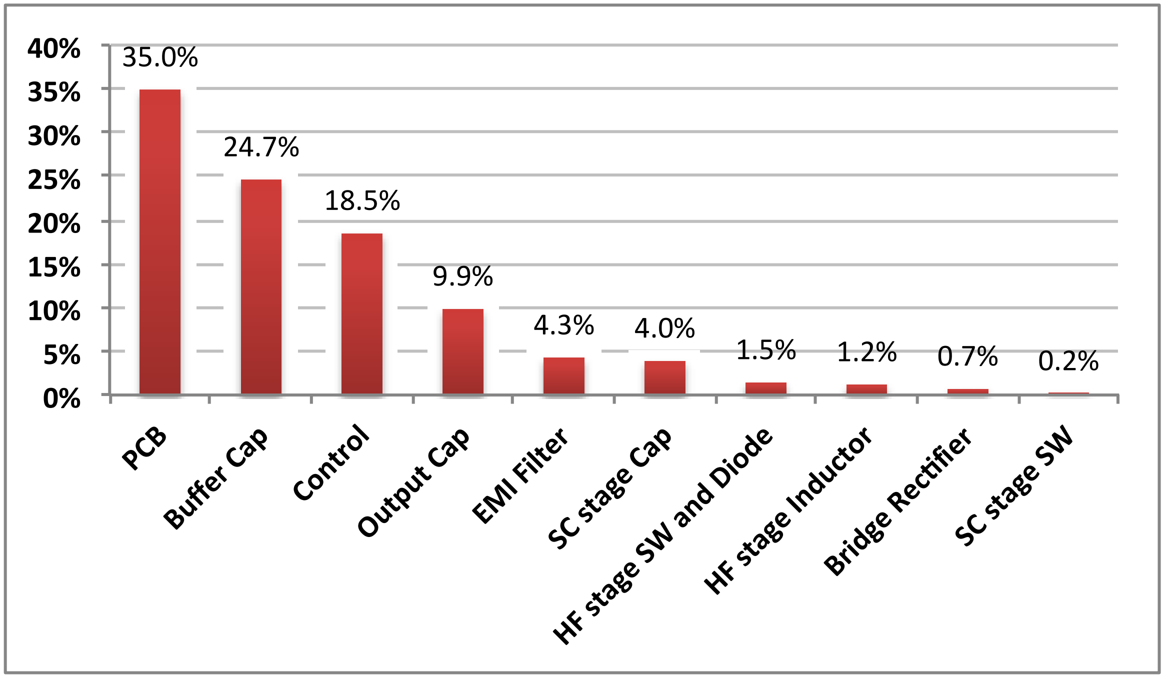
# EMI Performance




- **Meets FCC Class B EMI requirements with a small filter**
  - **EMI filter not optimized**
- **Measured ‘peak’ spectrum passes ‘quasi-peak’ limit**
  - **(Quasi-peak response is always less than or equal to peak response)**

# Prototype Power Density




- > 50 W/in$^3$ "box" power density
  - Displacement power density: 130 W/in$^3$
  - Logic / controls, pcb volume and layout can be further optimized and integrated
- ~10X power density improvement over commercial designs (for a ~100x frequency increase)

# Summary (1)

- **Greatly increased switching frequencies offer potential for substantial miniaturization**
  - **For grid interface, must still manage twice-line-frequency energy buffering**
- **Appropriate system design methods enable operation at HF and VHF frequencies (3-300 MHz)**
  - **At grid interface voltages one must overcome both loss and parasitic limits to achieve high frequency operation**
- **To push up frequencies at high $V_{in}$, moderate power:**
  - **Use “stacked” architectures to reduce subsystem voltages, $Z_o$**
  - **Utilize converter topologies with ZVS and low $Z_o$**

## Summary (2)

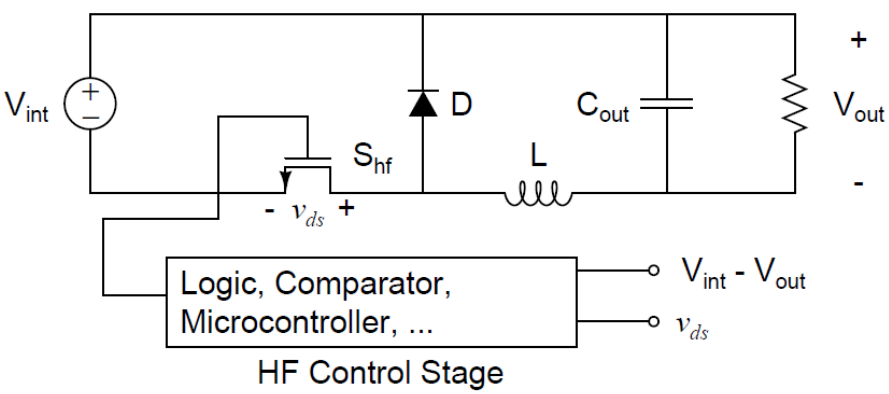
- **Feasibility and advantages of this approach has been demonstrated in a high-frequency (5-10 MHz) LED driver**
  - **~10 x power density for ~100 x frequency increase**
  - **High power factor (~0.88) without electrolytic capacitors**
  - **High efficiency (>90%)**
  - **EMI requirements can be met with small filters**

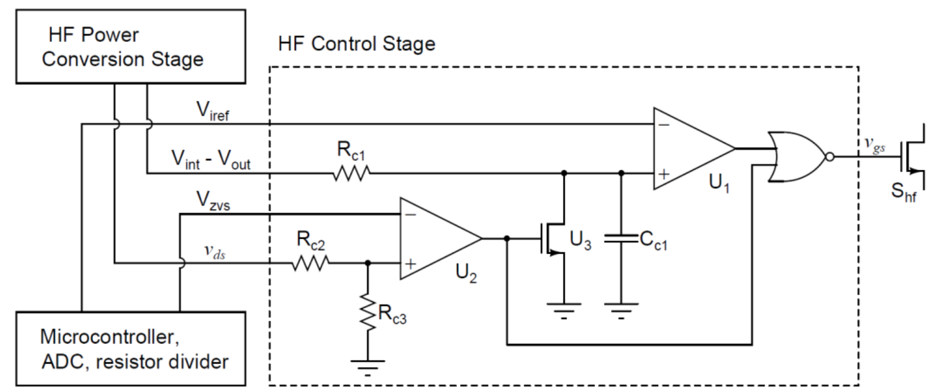
| | Typ. Commercial | Powerchip |
|---|---|---|
| Efficiency | 64 - 85 % | 92 % |
| Switching Frequency | 57 - 104 kHz | 5-10 MHz |
| Power Factor | 0.73-0.93 | 0.88 |
| Power Density | < 5 W/in$^3$ | > 50 W/in$^3$ |

# Acknowledgements


- **ARPA-E & Texas Instruments**
- **ARPA-E ADEPT PowerChip team members**
- **Co-authors of this work**
  - **Seungbum Lim**
  - **David Otten**

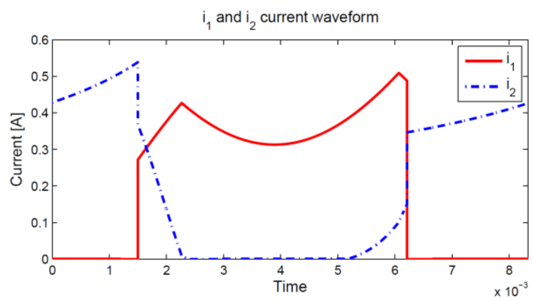
# HF Inverted Buck Converter Control

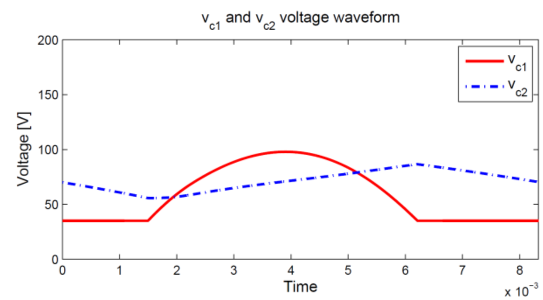


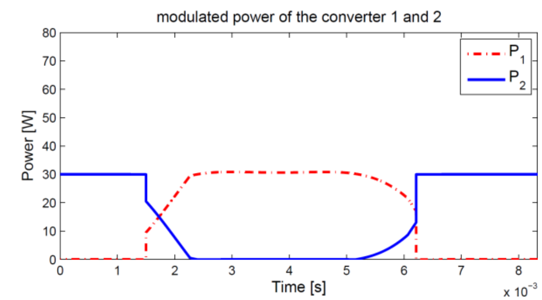



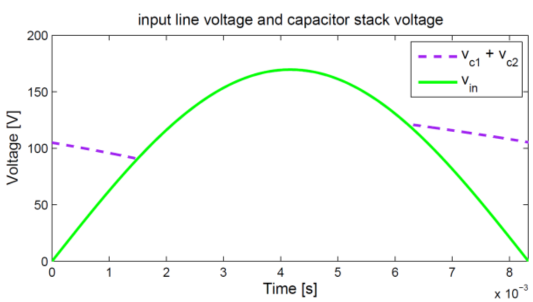

- **peak inductor current is controlled by changing switch on-time**
  - **Enables continuous modulation of power at high frequency**
- **turn on at ZVS / near ZVS voltage**

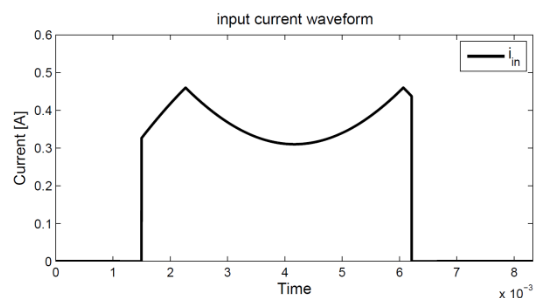
# Stacked Converter Model Simulation

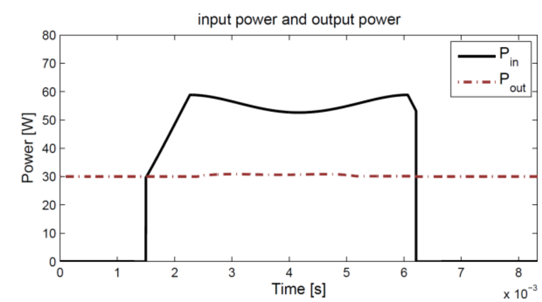



- **Example current and voltage waveforms**
- **For desired input power, calculate $i_1$ and $i_2$ currents over the ac line cycle (command for the individual dc-dc conversion blocks)**
- **Constant output power supplied to load**

# EMI Specifications

- **FCC part 15 subpart B Conducted limits**

**Class B**

| Frequency of emission [MHz] | Conducted limit (dBuV) | |
|---|---|---|
| | Quasi-peak | Average |
| 0.15 – 0.5 | 66 to 56 | 56 to 46 |
| 0.5 – 5 | 56 | 46 |
| 5 – 30 | 60 | 50 |

**Class A**

| Frequency of emission [MHz] | Conducted limit (dBuV) | |
|---|---|---|
| | Quasi-peak | Average |
| 0.15 – 0.5 | 79 | 66 |
| 0.5 – 30 | 73 | 60 |